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12. (New) A system for renaming source registers of instructions stored in an instruction window of a processor, wherein the instruction window comprises a plurality of storage locations each of which stores a single instruction and wherein only a subset of the plurality of storage locations may be filled with new instructions in a single processor cycle, the system comprising:

control logic that assigns one of a plurality of tags to a new instruction in the instruction window, each of said plurality of tags uniquely identifying a register for storing a result corresponding to an instruction in the instruction window;

a data dependency checker that determines if said new instruction is dependent on another instruction in the instruction window by comparing a source register address of said new instruction with a destination register address of said other instruction in the instruction window; and

tag assignment logic that outputs a renamed source register address for said new instruction, wherein said renamed source register address comprises a tag assigned to said other instruction in the instruction window if said new instruction is dependent on said other instruction.

13. (New) The system of claim 12, further comprising:

a first-in-first-out (FIFO) buffer that stores said plurality of tags;

wherein said control logic assigns a tag from a head of said FIFO buffer to said new instruction in the instruction window.

14. (New) The system of claim 13, wherein said FIFO buffer comprises:

a plurality of slots equal in number to a predetermined size of the instruction window, each of said plurality of slots containing a unique one of said plurality of tags, wherein an order defined by positions of said plurality of tags in said FIFO buffer corresponds to an order of instructions in the instruction window.

15. (New) The system of claim 12, further comprising:

a register file that stores a source register address and a destination register address for each instruction in the instruction window, said register file coupled to said

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data dependency checker for providing said source register address of said new instruction and said destination register address of said other instruction in the instruction window to said data dependency checker.

16. (New) The system of claim 12, wherein said data dependency checker comprises:

a compare circuit that compares said source register address of said new instruction with said destination register address of said other instruction in the instruction window.

17. (New) The system of claim 12, further comprising:

a register file comprising a write data port and a write address port;
wherein said tag assignment logic stores said renamed source register address in said register file by providing said renamed source register address to said write data port and providing said tag associated with said new instruction to said write address port.

18. (New) The system of claim 17, wherein said register file further comprises:

a read data port and a read address port;
wherein said renamed source register address stored in said register file is accessed on said read data port by providing said tag associated with said new instruction to said read address port.

19. (New) The system of claim 12, further comprising:

a retirement unit that determines whether said new instruction has retired.

20. (New) The system of claim 19, further comprising:

logic that selects one of said register source address of said new instruction or said renamed register source address based on whether said new instruction has retired.
